

	Document ID	Issue Date	Pages	Title	Current OR
1	US 20040133871 A1	20040708	15	Matrix optical process correction	716/19
2	US 20040115539 A1	20040617	25	Method of achieving CD linearity control for full-chip CPL manufacturing	430/5
3	US 20040107412 A1	20040603	21	Method and system for context-specific mask writing	716/19
4	US 20040067423 A1	20040408	24	Hybrid phase-shift mask	430/5
5	US 20040053158 A1	20040318	48	Onium salts and the use thereof as latent acids	430/270.1
6	US 20040044984 A1	20040304	18	Considering mask writer properties during the optical proximity correction process	716/21
7	US 20040013952 A1	20040122	10	Method for structuring a lithography mask	430/5
8	US 20030233630 A1	20031218	29	Methods and systems for process control of corner feature embellishment	716/19
9	US 20030192013 A1	20031009	13	Method and apparatus for facilitating process-compliant layout optimization	716/2
10	US 20030188283 A1	20031002	15	Method and apparatus for identifying an identical cell in an IC layout with an existing solution	716/11
11	US 20030180632 A1	20030925	12	Mask for use in lithography, method of making a mask, lithographic apparatus, and device manufacturing method	430/5

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12	US 20030177465 A1	20030918	16	Using a suggested solution to speed up a process for simulating and correcting an integrated circuit layout	716/11
13	US 20030126581 A1	20030703	56	User interface for a network-based mask defect printability analysis system	716/19
14	US 20030079194 A1	20030424	41	Method of automatic layout design for LSI, mask set and semiconductor integrated circuit manufactured by automatic layout design method, and recording medium storing automatic layout design program	716/8
15	US 20030068566 A1	20030410	13	Full phase shifting mask in damascene process	430/5
16	US 20030023939 A1	20030130	19	METHOD AND APPARATUS FOR ANALYZING A LAYOUT USING AN INSTANCE-BASED REPRESENTATION	716/3
17	US 20020182514 A1	20021205	16	Organic bottom antireflective coating for high performance mask making using optical imaging	430/5
18	US 20020100005 A1	20020725	17	Integrated verification and manufacturability tool	716/5
19	US 20020028390 A1	20020307	35	TECHNIQUES FOR FABRICATING AND PACKAGING MULTI-WAVELENGTH SEMICONDUCTOR LASER ARRAY DEVICES (CHIPS) AND THEIR APPLICATIONS IN SYSTEM ARCHITECTURES	430/5
20	US 20020015899 A1	20020207	24	Hybrid phase-shift mask	430/5
21	US 20010052107 A1	20011213	17	Integrated verification and manufacturability tool	716/4

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22	US 20010036591 A1	20011101	35	Iodonium salts as latent acid donors	430/270.1
23	US 6777170 B1	20040817	39	Stereolithographic patterning by variable dose light delivery	430/320
24	US 6757645 B2	20040629	38	Visual inspection and verification system	703/13
25	US 6753131 B1	20040622	37	Transparent elastomeric, contact-mode photolithography mask, sensor, and wavefront engineering element	430/322
26	US 6745372 B2	20040601	13	Method and apparatus for facilitating process-compliant layout optimization	716/2
27	US 6730256 B1	20040504	39	Stereolithographic patterning with interlayer surface modifications	264/401
28	US 6664009 B2	20031216	19	Method and apparatus for allowing phase conflicts in phase shifting mask and chromeless phase edges	430/5
29	US 6623895 B2	20030923	23	Hybrid phase-shift mask	430/5
30	US 6605394 B2	20030812	15	Organic bottom antireflective coating for high performance mask making using optical imaging	430/5
31	US 6578188 B1	20030610	57	Method and apparatus for a network-based mask defect printability analysis system	716/19
32	US 6571383 B1	20030527	11	Semiconductor device fabrication using a photomask designed using modeling and empirical testing	716/19
33	US 6569575 B1	20030527	15	Optical lithography beyond conventional resolution limits	430/5

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34	US 6560766 B2	20030506	20	Method and apparatus for analyzing a layout using an instance-based representation	716/19
35	US 6556702 B1	20030429	39	Method and apparatus that determines charged particle beam shape codes	382/144
36	US 6546540 B1	20030408	39	Method of automatic layout design for LSI, mask set and semiconductor integrated circuit manufactured by automatic layout design method, and recording medium storing automatic layout design program	716/13
37	US 6428940 B1	20020806	18	Method for pattern generation with improved image quality	430/22
38	US 6421820 B1	20020716	19	Semiconductor device fabrication using a photomask with assist features	716/21
39	US 6415421 B1	20020702	15	Integrated verification and manufacturability tool	716/4
40	US 6379868 B1	20020430	17	Lithographic process for device fabrication using dark-field illumination	430/311
41	US 6306555 B1	20011023	32	Iodonium salts as latent acid donors	430/270.1
42	US 6233044 B1	20010515	45	Methods and apparatus for integrating optical and interferometric lithography to produce complex patterns	355/67

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43	US 6114071 A	20000905	12	Method of fine feature edge tuning with optically-halftoned mask	430/5
44	US 5942374 A	19990824	20	Integrated circuits formed in radiation sensitive material and method of forming same	430/312
45	US 5821014 A	19981013	14	Optical proximity correction method for intermediate-pitch features using sub-resolution scattering bars on a mask	430/5
46	US 5759744 A	19980602	27	Methods and apparatus for lithography of sparse arrays of sub-micrometer features	430/312
47	US 5691089 A	19971125	20	Integrated circuits formed in radiation sensitive material and method of forming same	430/5
48	US 5666189 A	19970909	19	Process for performing low wavelength photolithography on semiconductor wafer using afocal concentration	355/53

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49	US 5591564 A	19970107	20	Gamma ray techniques applicable to semiconductor lithography	430/311
50	US 5580687 A	19961203	88	Contact stepper printed lithography method	430/5
51	US 5567570 A	19961022	19	Gamma ray techniques applicable to semiconductor lithography	430/311
52	US 5567550 A	19961022	19	Method of making a mask for making integrated circuits	430/5
53	US 5554484 A	19960910	18	Gamma radiation sensitive resist materials for semiconductor lithography	430/270.1

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54	US 5512395 A	19960430	19	Image masks for semiconductor lithography	430/5
55	US- 5309354 A	19940503	24	Electron beam exposure method	700/57
56	US 5306584 A	19940426	8	Mask or wafer writing technique	430/5
57	US 5246800 A	19930921	16	Discrete phase shift mask writing	430/5
58	US 5055383 A	19911008	10	Process for making masks with structures in the submicron range	430/312
59	US 4022928 A	19770510	17	Vacuum deposition methods and masking structure	430/296